II-5. A 1200 MEGABITS/SEC, GRAY CODE, ANALOG TO DIGITAL CONVERTER

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This paper considers a novel 9 GHz microwave carrier system which can sample a baseband analog input signal at a 200 MHz rate and encode into Gray Code 6-bit words (64 levels), giving a bit rate of 1200 megabits/second. This performance is obtained through the use of a system employing the microwave counterpart of a serial type Gray coder first described by B. D. Smith[1]. In this new system the baseband analog signal amplitude is replaced by microwave carrier amplitude, while baseband analog signal polarity is replaced by microwave carrier phase.

Baseband System. Consider Smith's original encoder which comprises a tandem connection of N nonlinear networks, each having an analog and a dc reference input, and a digit and an analog residue output. The system produces an N digit Gray code at its digital output terminals. A typical nonlinear network shown in Figure 1a, may be characterized by the input-output characteristic shown in Figures 1b and 1c. Fig. 1b shows the analog input signal E_1 located on the x-axis such that its midpoint is at zero voltage. The digit output voltage E_D is such that $E_D = 1$ when $E_1 > 0$, and $E_D = 0$ when $E_1 < 0$.

In Fig. 1c the output E_2 (residue) is related to the input E_1 by: $E_2 = E_{ref} - 2\,|E_1|$. This results in the "inverted V" transfer function which is characteristic for this type of Gray encoder. When N of these stages are cascaded, with the output E_2 of one stage being the input E_1 of the succeeding stage, an N digit Gray code will appear at the digit output.

Microwave System. Let the aforementioned analog signal E_1 modulate a cw microwave carrier. Let the modulation be done by a conventional AM balanced modulator. Then the output signal will be a double sideband suppressed carrier wave. Let E_1 be the analog input signal, and represent the microwave carrier as $\cos(\omega_c t+\varphi)$, where φ denotes the carrier phase. If we arbitrarily let $\varphi = \pi$ radians, then the modulator output signal will be of the form:

$$E_2 = |E_1| \cos(\omega_c t + \pi) \qquad (1)$$

Now when: $E_1 > 0$, $\quad E_2 = |E_1| \cos(\omega_c t + \pi) \qquad (2)$

$E_1 < 0$, $\quad E_2 = -|E_1| \cos(\omega_c t + \pi) \qquad (3)$

The above equations imply that the envelope height (magnitude) of E_2 is proportional to the magnitude of E_1 and the E_2 carrier phase depends upon the polarity of E_1, where n phase represents + polarity and vice versa.

In Fig. 2a tha balanced modulator is shown cascaded with the first stage of an N-stage microwave Gray encoder. Fig. 2b, a graphical representation of Eq. (1), shows E_2 the modulator output vs. E_1 the analog input, where the magnitude of E_2 is represented by the distance of the curve from the x-axis, and the phase of E_2 is represented by the quadrant in which the curve lies -- quadrants 1 and 2 represent π phase and quadrants 3 and 4 represent 0 phase.

Fig. 2c shows E_3, the output signal from the stage 1 coder. Note that E_3 differs from E_2 only in that the carrier phase has been shifted π radians when $E_1 > 0$, or,

$$E_3 = |E_1| \cos \omega_c t \tag{4}$$

E_3 is related to E_2 by:

$$\begin{aligned} E_3 &= E_2 \quad \text{when } \varphi(E_2) = 0 \\ E_3 &= -E_2 \quad \text{when } \varphi(E_2) = \pi \end{aligned} \tag{5}$$

Fig. 2d results when E_3 is "sliced" by adding a reference cw carrier,

$$E_{ref} = \left| \frac{E_{1\,max}}{2} \right| \cos(\omega_c t + \pi)$$

This makes:

$$E_4 = E_3 + E_{ref} \tag{6}$$

or,

$$E_4 = \left(\left| \frac{E_{1\,max}}{2} \right| - |E_1| \right) \cos(\omega_c t + \pi) \tag{7}$$

where E_4 is the input signal to the stage 2 coder. Note that E_4 has the familiar "inverted V" shape discussed earlier, which is characteristic of the Gray code. Hence, Fig. 2 represents the microwave carrier counterpart of Smith's[1] baseband coder where carrier phase has been substituted for baseband polarity.

Fig. 2e shows the digit output E_D available from the stage 1 coder:

$$\begin{aligned} E_D &= -1 \quad \text{when } \varphi(E_2) = 0 \\ E_D &= 1 \quad \text{when } \varphi(E_2) = \pi \end{aligned} \tag{8}$$

Microwave Circuitry. Figure 3 shows a method of realizing the scheme set forth in Fig. 2. In particular, we concentrate on the apparatus represented by the box called "Stage 1" in Fig. 2a. Let E_2 (Fig. 3) be the balanced modulator output and Stage 1 input. Now a prime function of Stage 1 is to decide the phase of E_2. If E_2 has π phase, then the system must emit a digit 1 ($E_D = 1$) output and shift E_3 to 0 phase. Alternatively, if E_2 has 0 phase, the system must emit a digit 0 ($E_D = -1$) output and keep E_3 at 0 phase. This is done by first diverting a portion of E_2 through a directional coupler, then passing this signal through a high gain (50 dB) amplifier, limiter, and synchronous detector. If the local oscillator voltage driving the detector has the correct phase α, then the baseband output signal E_D will have positive polarity when E_2 has n phase and negative polarity when E_2 has 0 phase. A portion of E_D may be diverted off as the baseband digit output. The remainder is used to switch a two-state varactor diode digital reflection-type phase shifter that appropriately shifts the phase of E_2 to generate E_3. If a coherent cw carrier of correct magnitude and phase is now added to E_3, the output signal E_4 will be formed. When six of these microwave stages are cascaded, with the output E_4 of one stage being made the input E_2 of the succeeding stage, a six-digit Gray code will appear at the E_D output terminals.

Acknowledgment. The author acknowledges the support and encouragement of Mr. M. R. Barber.

Reference. 1. B. D. Smith, "An Unusual Electronic Analog-Digital Conversion Method", IRE Trans. Instrumentation, pp 155-160, June 1956.

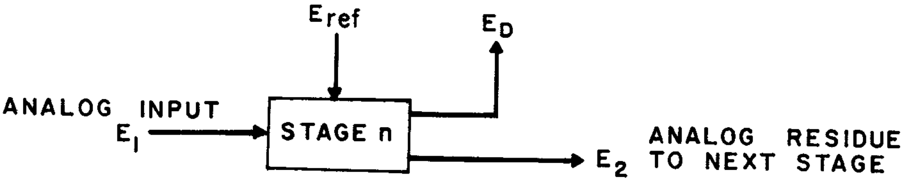

Figure 1a. Baseband Coder Schematic

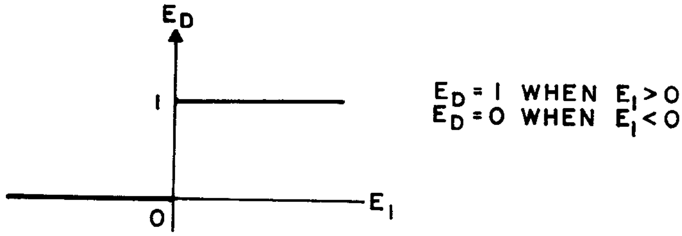

Figure 1b. Digit Output vs. Analog Input

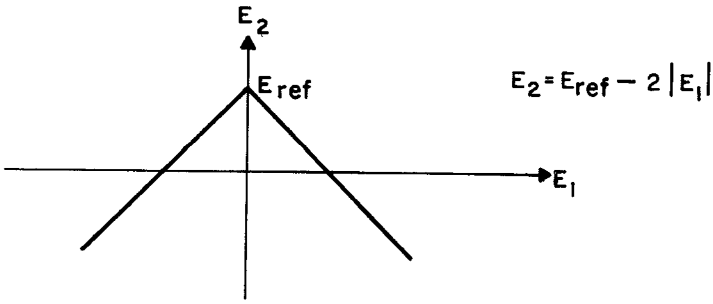

Figure 1c. Analog Residue Output vs. Analog Input

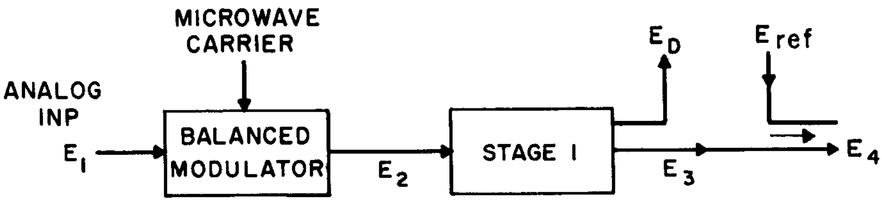

FIG. 2-a CODER SCHEMATIC

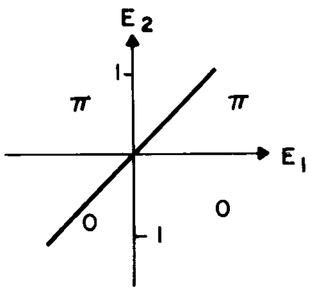

FIG. 2-b

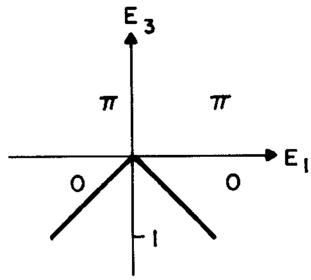

FIG. 2-c

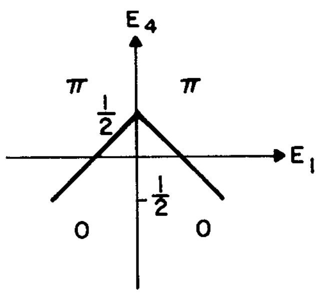

FIG. 2-d

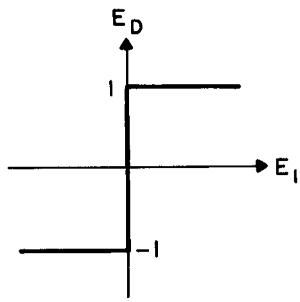

FIG. 2-e

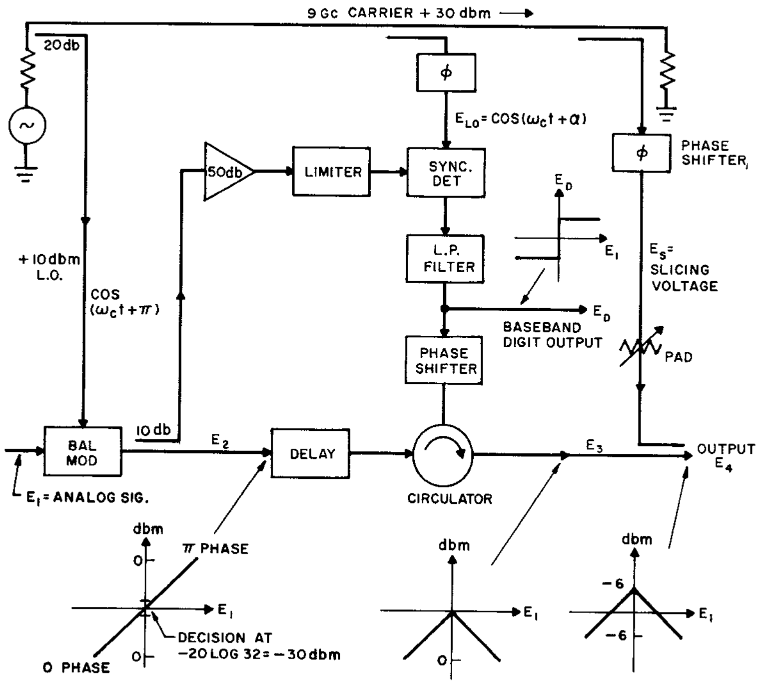

FIG.3 A/D CONVERTER–STAGE I 6 BIT SYSTEM